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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/022,123	12/13/2001	Sifen Luo	US 010624	2515

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EXAMINER	
NGUYEN, LINH V	
ART UNIT	**PAPER NUMBER**
2819	

DATE MAILED: 02/24/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/022,123	LUO ET AL.	
	Examiner	Art Unit	
	Linh V Nguyen	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 December 2003*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) _____ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Prior Art of Record

Admission Prior Art Fig. 2, and 3 common owned with this application may constitute prior art, if prior art is 102(b).

Claim Rejections - 35 USC § 112

1. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. Claims 1, 7, 11, 18 and 21, are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter, which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. The subject matter "sense corrector current (or drain) current in an input stage transistor", which was not described nowhere in the specification.

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 1, 7, 11, 18 and 21, are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention, because under description of Fig. 1, and Fig. 1A of the invention disclosing multiple transistors in the input amplifier stage, and applicant fails to point out which transistor needs to be sense.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

6. Claims 1 - 26, are rejected under 35 U.S.C. 102(e) as being anticipated by Shinjo et al. Pub. No.: 2003/0048135 A1.

Regarding to claim 1, Figs. 2 – 5, of Shinjo et al. disclose an multi-stage RF power amplifier circuit having at least an input stage (12-1) and multiple output stages (12 [N-1], 12[N], 13[N]) for amplifying an input signal (1) comprising: sensing a collector or drain current in an input stage transistor (Fig. 3[23] disclosing collector current of transistor 33 to current adding circuit 24 in the input stage of 12-1 of Fig. 2) or drain (is an alternative limitation for different type of transistor only); feeding a current equal or proportional to said input stage transistor collector current (Fig. 4 discloses circuit of 24) to an output stage bias circuit (Fig. 2[25], See Fig. 5) to boost the bias of an output

stage (Fig. 2 [12-(N-1)], See Page 3, lines 6 – 11 of paragraph [0046]); wherein the input stage transistor is operated in a class AB mode (See Page 4 paragraph [0053]), and said output stage is fed through a matching network (Fig. 2[11-N]).

Regarding to claim 2, wherein the input stage transistor collector current (Fig. 3 [23])) is sensed (Fig. 2[24]) and fed to the output stage bias circuit (25) via a current mirror (Figs. 3 and 4).

Regarding to claim 3, wherein one transistor comprising said current mirror is connected in series with a transistor that itself forms a second current mirror with the input stage transistor (Figs. 3 and 4).

Regarding to claim 4, wherein the amplifier circuit comprises plural bipolar junction transistors (Figs 3, 4, 5).

Regarding to claim 5, wherein the amplifier circuit comprises plural field effect transistors (Fig. 2).

Regarding to claim 6, wherein the amplifier circuit comprises a combination of BJTs and FETs (Figs. 2 – 5).

Regarding to claim 7, Figs. 2 – 6 of Shinjo et al. disclose a multi-stage power amplifier circuit comprising: an input stage (12-1); an output stage (12 [N-1], 12[N], 13[N])) for amplifying in put signal (1) comprising: an input stage having an input stage transistor (Fig. 3); an output stage biasing circuit (25); and a current mirror (Fig. 4), which senses collector or drain current of said input stage transistor (Fig. 3) and feeds a current proportional to said input signal current to said output stage biasing circuit (25).

Regarding to claim 8, wherein said current mirror includes at least one BJT (Figs. 3 - 5).

Regarding to claim 9, wherein said current mirror includes at least one FET (Figs. 2).

Regarding to claim 10, wherein said transistor comprised within said circuit includes both BJTs and FETs (Figs 2 – 6).

Regarding to claims 11 – 20, Figs. 2 – 6 of Shinjo et al. as applied to claims 1 – 10 above, disclosed every aspect of applicant claims invention.

Regarding to claim 21, Figs. 2 – 6 of Shinjo et al. disclose a bias boosting sub-circuit (25) for a multi-stage power amplifier circuit (Fig. 2 [12-1,...12 N.. 13-N) for amplifying an input signal (1), said multistage power amplifier comprising at least an input stage (12-1) and an output stage (12-(N-1), 12-N, 13-N), said sub-circuit comprising: two matched BJTs in a first current mirror (Fig. 3 [32,33] of 23 in Fig.2), wherein the first current mirror senses a collector (Fig. 3[23] disclosing collector current of transistor 33 to current adding circuit 24 in the input stage of 12-1 of Fig. 2) or drain (is an alternative limitation for different type of transistor only) current of an amplifying transistor in the input stage (12-1), and feeds an equal or proportional current to a bias circuit (Fig. 4) of the output stage (Fig. 2).

Regarding to claim 22, wherein one of the transistors of the first current mirror is connected in series with a third transistor, said third transistor itself forming a second current mirror with the input stage-amplifying transistor (Fig. 4 [41,42]).

Regarding to claim 23, wherein one transistor of the first current mirror comprises two matched PNP BJTs, and the second current mirror comprises two matched NPN BJTs (Figs. 3 – 5).

Regarding to claim 24, where one transistor of the first current mirror has its collector connected to a collector of the third transistor (Figs 3 and 4).

Regarding to claim 25, the subcircuit further transistors and wherein a collector current mirror and is connected to a collector of an NPN transistor in the output stage (Fig. 4 – 5).

Regarding to claim 26, wherein the NPN transistor is a current mirror (Fig. 5).

Response to Arguments

7. Applicant's arguments filed 12/08/03 have been fully considered but they are not persuasive.

With respect to claims 1, 7, 11, 18 and 21, under remark applicant argued that "Shinjo does not teach or disclose "sense corrector current (or drain) current in an input stage, which is one of the multiple stages for amplifying an input signal", examiner is respectful disagree from the following:

Figure 2 of Shinjo disclose an amplifier circuit having multiple input and output stages (2) for amplifying input signal 1; wherein the input stage 12-1 of 2 having detection circuit 23, current adding circuit 24, and bias circuit 25 to boost the output stages 12-(N-1), 12 – N; wherein the detection circuit 23 of the input stage 12-1 having a collector current (See Fig. 3 [33]) which is sensed by the circuit 24, and provided a

proportion current to bias circuit (25) to boost the multiple output stages (See Page 3, lines 6 – 11 of paragraph [0046]).

Conclusion

8. THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

5. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Linh Van Nguyen whose telephone number is (571) 272-1810. The examiner can normally be reached from 8:30 – 5:00 Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mr. Michael Tokar can be reached at (571) 272-1812. The fax phone numbers for the organization where this application or proceeding is assigned are (703-872-9306) for regular communications and (703-872-9306) for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

LVN

February 11, 2004

Michael J. Tokar

Michael Tokar
Supervisory Patent Examiner
Technology Center 2800